REMARKS

Upon entry of this amendment, claims 47-52 will be pending in the application. Claim 47 was amended to require that the device layer comprises a region which comprises the axis and has a radial width of at least 7.5% of the radius is which is free of agglomerated vacancy defects and to amplify the fact that the region which is substantially free of agglomerated vacancy defects is a vacancy dominated region. Claim 52 has been added by this amended. Support for the amendment to claim 47 and for new claim 52 can be found, for example, at page 33, line18 through page 34 line 1 of the specification.

Although Applicant maintains that the subject matter of claim 47, as originally presented, is patentable over the disclosure of Nakato et al. and Hourai et al., Applicant has nevertheless presented the amendments herein in the interest of advancing prosecution.

Objection to claim 51

According to Applicant's records, Claim 51, as added in Preliminary Amendment A, requires the wafer be annealed at temperatures of 800°C and 1000°C and not at 8000C and 1000C as stated in the office action. In any event, claim 51 has been amended to ensure that it includes the proper numerical values and degree symbol.

Obvious-type Double Patenting

Applicant has enclosed herewith a Terminal Disclaimer in accordance with 37 CFR 1.130(b) and 37 CFR 321(c) thereby obviating the obvious-type double patenting rejection of claims 47-51 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 17-20, 27, 30 and 38 of United States Patent No. 6,236,104 and claims 1, 7 and 40-42 of U.S. Patent No. 6,342,725. Accordingly, Applicant requests the rejection be withdrawn.

Patentability of Amended Claims 47-51 over Nakato et al in view of Hourai et al.

Claim 47, as amended, is directed to a silicon on insulator (hereinafter SOI) structure having a device layer, a single crystal silicon handle wafer and an insulating layer between the device layer and the handle wafer. According to Claim 47, the device layer comprises an axially symmetric region **which is vacancy dominated and substantially free of agglomerated intrinsic point defects** and which comprises the central axis and has a radial width of at least about 7.5% of the radius of the device layer.

Nakato et al. (U. S. Patent No. 5,436,175) describe an SOI structure having a device layer, a single crystal silicon handle wafer and an insulating layer between the device layer and the handle wafer. The Office acknowledges that Nakato et al. do not describe or suggest an SOI structure having a device layer having the characteristic features of claim 47 and relies on the disclosure of Hourai et al. to fill the deficiencies of Nakato et al.

Hourai et al. (Japanese Patent Application No. 8-330316, now Japanese Patent No. 3085146)[1] describe a process in which v/G is controlled to within a vary narrow range to produce a silicon wafer and ingot which is free of infrared light scattering defects, oxidation induced stacking faults and dislocation clusters. Hourai et al. fail to disclose or suggest a silicon wafer or ingot having an axially symmetric region **which is both vacancy dominated and substantially free of agglomerated intrinsic point defects**. That is, Hourai et al. describe a wafer and ingot which are produced entirely

[1]Applicant's comments and references regarding Hourai et al.'s Japanese Patent Application No. 8-330316 are based on the English translation submitted during the prosecution of prior U. S. Patent Application No. 09/387,288, now U. S. Patent No. 6,236,104, from which the present application claims priority. A copy of the translation of Japanese Patent Application No. 8-330316 is attached for the Examiner's convenience.

within a region described by Hourai et al. to be a "no-defect" region. Significantly, the "no-defect" region described by Hourai et al. cannot be vacancy dominated for two reasons. First, the "no-defect" region cannot be vacancy dominated because Hourai et al. explicitly describe their wafer as being a low pulling rate wafer, and their process as being a low pulling rate process which as discussed in more detail below implies that the material is grown under interstitial dominated growth conditions. Second, Hourai et al. subjected material having this "no-defect" region to a standard oxygen precipitation heat treatment, and no defects were formed in the "no-defect" region. It is well established that if vacancy dominated defect free material exists in a silicon wafer, it will precipitate oxygen when subjected to an oxygen precipitation heat treatment.[2] Thus, although Hourai et al. disclose a wafer and ingot which are purported to be "no-defect" material, they do not disclose or suggest a wafer or ingot having a region which is both vacancy dominated and defect free. In fact Hourai et al. describe a process for producing interstitial dominated material.

The Hourai et al. process is a low pulling rate process which yields interstitial dominated wafers. Hourai et al. describe their invention as being a low pulling rate wafer:

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[2] "Simulation of the Point Defect Diffusion and Growth Condition For Defect Free CZ Silicon Crystal," Nakamura et al., Electrochemical Society Proceedings Volume 2002-2, p. 554 (2002). Nakamura et al. subjected an axial slice of a Czochralski grown silicon ingot to a thermal anneal at 780 °C for 3 hr and at 1000 °C for 16 hr and observed the oxygen precipitation by X-ray topography. Nakamura observed two regions with and without oxygen precipitates between the OSF ring and B-band (a type of agglomerated intrinsic point defect) and state that the boundary between the two regions is the boundary between vacancy dominated material and interstitial dominated material. Oxygen precipitation appears on the vacancy side of the boundary and no oxygen precipitation appears on the interstitial side of the boundary. See page 555, line 32 through page 557, line 12-17.

> **Wafers of this inv ntion are of low pull rate**; OISF ring disappears at the axis; no OISFs nor LSTDs are present which occur inside this ring; dislocation clusters are not present which occur outside the ring; thus high quality wafers are obtained without any harmful defects in whole wafer.[3] (emphasis added)

Elsewhere in the specification, Hourai et al. define a "low pulling rate wafer" as wafers pulled at a rate of 0.5 mm/min. or less; pulling rates of 0.5-0.8 mm/min. are considered "medium" and pulling rates in excess of 0.8 mm/min. are considered "high."[4]

Hourai et al. describe and illustrate the differences between low, medium and high pulling rate silicon single crystal. High pulling rates lead to the formation of an OSF ring at the outermost periphery of the single crystal and the formation of LSTDs inside the ring.[5] The effect of medium pulling rates is illustrated in Figs. 1A and 1B; single crystal silicon grown at these rates has an OSF ring developing region at approximately one-half of the radius (Fig. 1A) or at the center of the wafer (Fig. 1B) and, depending upon the position of the OSF ring, infrared scattering defects inside the OSF ring (Fig. 1A) or dislocation clusters outside the OSF ring (Fig. 1A). On the other hand, when the pull rate is lowered to less than 0.5 mm/min, the ring disappears at the radial center, and the LSTD defect region inside the ring disappears. "But dislocation clusters are formed in whole wafer to degrade the device characteristics and to lower IG ability. Therefore, the low pull rate wafers are not suitable for the high level integration

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[3] English translation of Japanese Application No. 8-330316, paragraph [0031].

[4] English translation of Japanese Application No. 8-330316, paragraphs [0005] through [0015].

[5] English translation of Japanese Application No. 8-330316, paragraph [0026].

device applications."[6] Dislocation clusters, cannot form unless, prior to the agglomeration reaction, silicon self-interstitials are the predominant intrinsic point defect.[7] **When Hourai et al. state that dislocation clusters develop all over the wafer, they are also stating that silicon self-interstitials are the predominant intrinsic point defect all over their wafer**. Therefore, when Hourai et al. describe their invention as being a low pulling rate wafer, it is implicit that the wafer have silicon self-interstitials as the predominant intrinsic point defect across the entire diameter of the wafer.

The "no-defect" region described by Hourai et al does not precipitate oxygen. As noted above, it is well established that vacancy dominated material substantially free of agglomerated defects exhibits a high concentration of oxygen precipitates after being subjected to oxygen precipitation heat treatments. For example, Fig. 26B of the present application shows an image of an axial slice of an ingot taken after subjecting the slice to an oxygen precipitation heat treatment. The region along the axis from 290 mm to 400 mm has an axially symmetric region of interstitial dominated material free of agglomerated intrinsic point defects surrounding a generally cylindrical core of vacancy dominated material which is also free of agglomerated intrinsic point defects.[8] Significantly, the vacancy dominated region located inside the V/I boundary exhibits substantial oxygen precipitation appearing as a light colored (white/gray) region, whereas the interstitial dominated region does not exhibit oxygen precipitation and appears as a dark or black region.

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[6] English translation of Japanese Application No. 8-330316, paragraphs [0008] through [0015].

[7] Specification of the present application at page 2, line 4 through page 3, line 7.

[8] Specification of the present application at page 52 line 25 through page 53 line 2.

According to Hourai et al., after subjecting the axial slice depicted in figure 4 to a thermal treatment in dry oxygen at 800 °C for 4 hours and at 1000 °C for 16 hours and examining the sample by X-ray topography, no defects are observed in the "no-defect region".[9] That is, no oxygen precipitates form. Significantly, vacancy dominated material forms oxygen precipitates upon being subjected to an oxygen precipitation heat treatment as described above, thus the "no-defect region" described in figure 4 of Hourai et al., **cannot include any vacancy dominated material**. Hourai et al. explicitly state that the defect distributions shown in figure 4 correspond to the calculated results shown in figure 3 used to determine the range of v/G values required by the Hourai et al. process. That is, Hourai et al. disclose a process for growing an ingot wherein v/G is maintained within the range of values corresponding to the "no-defect region" shown in figure 3 and 4 over the entire radius and along the entire axial length. Thus, Hourai et al. fail to describe any silicon having the characteristics of the device layer in the SOI structure of claim 47, as amended, since Hourai et al. fail to describe or suggest any silicon which is vacancy dominated and substantially free of agglomerated intrinsic point defects and as such cannot cure the deficiencies of Nakato et al.

Claims 48-51 depend from claim 47 and are therefore submitted as patentable for the same reasons discussed above with respect to claim 47.

Claim 49 is further distinguishable over the cited references in that claim 49 requires that the handle wafer of the SOI structure have a non-uniform concentration of crystal lattice vacancies with the concentration in the bulk layer being greater than the concentration in the surface layer. According to claim 49, the vacancy profile is such that, if the structure were subjected an oxygen precipitation heat treatment, oxygen precipitates would form in the bulk of the handle wafer and a denuded zone would form in the surface layer of the handle wafer.

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[9]English translation of Japanese Application No. 8-330316, paragraph [0040].

None of the cited references disclose or suggest any wafer having a non-uniform vacancy concentration and certainly do not disclose or suggest the non-uniform vacancy concentration of claim 49. In rejecting claim 49, the Office has asserted that the formation of crystal lattice vacancies is inherent in the process disclosed by Nakato et al. It is well settled, however, that the Office must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.[10] The Office asserts that the non-uniform vacancy profile is somehow an inherent characteristic of the SOI substrate under thermal anneal following the implantation.

As discussed in the present application, the non-uniform concentration of crystal lattice vacancies described in claim 49 may be formed by thermally annealing a wafer at a temperature in excess of 1150°C under certain atmospheric conditions and then rapidly cooling the wafer at a rate of at least about 5°C/sec. The thermal anneal described in Nakato et al. will not invariably form any crystal lattice vacancies and to the extent any form, will not invariably form a non-uniform profile. Significantly, the thermal anneal described in Nakato et al. is carried out at a temperature in the range of 1100°C to 1400°C; as discussed in the present application, crystal lattice vacancies form at temperatures in excess of 1150°C. Therefore, the thermal anneal described in Nakato et al. may not form any vacancies at all if carried out at the lower end of the temperature range taught. Moreover even if the thermal anneal described in Nakato et al. was carried out at temperatures greater than 1150°C, the anneal process would not invariably form a non-uniform vacancy profile. As described in the present application, the process for preparing a non-uniform vacancy profile requires rapidly cooling the annealed wafer. Nakato et al. fail to describe or suggest rapidly cooling their wafer and, in fact, fail to even mention the rate at which their wafer is cooled.

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[10] M.P.E.P. §2112 and the references cited therein.

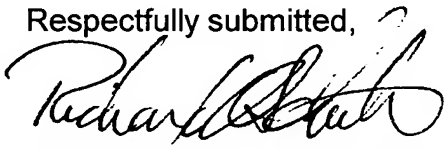
Claims 50 and 51 further require that the interstitial oxygen concentration profile in the handle wafer has certain characteristics. The Office has made no attempt to provide any basis in fact and/or technical reasoning to reasonably support the determination that these characteristics necessarily flow from the teachings of either Nakamura et al. or Hourai et al.

The Office's assertion that the phrase "such that upon subjecting the silicon wafer to an oxygen precipitation heat treatment..." constitutes a product by process limitation is simply incorrect. This phrase imposes a compositional and not a product by process requirement. More specifically, the claim requires that the handle wafer have a particular vacancy profile. The heat treatment merely reveals the claimed vacancy profile since oxygen precipitates form according to this template. As such, it is not a **product by process** limitation.

CONCLUSION

A check in the amount of $ 950.00 for a three month extension of time is enclosed. The Commissioner is hereby authorized to charge any under payment or credit any over payment to Deposit Account No. 19-1345.

Respectfully submitted,



Richard A. Schuth, Reg. No. 47,929
SENNIGER, POWERS, LEAVITT & ROEDEL
One Metropolitan Square, 16th Floor
St. Louis, Missouri 63102
(314) 231-5400

RAS/EJH/msc
*Enclosures

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